HIGH-PERFORMANCE GaAs HETEROJUNCTION BIPOLAR TRANSISTOR LOGARITHMIC IF AMPLIFIER

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ABSTRACT

The GaAs/AlGaAs heterojunction bipolar transistor (HBT) has been used to demonstrate a high performance logarithmic amplifier, also believed to be the first using the HBT technology. A "true" logarithmic intermediate frequency (IF) amplifier is implemented, based on a silicon bipolar transistor dual-gain log stage design. The HBT true log IF amplifier monolithically integrates four log stages to achieve a piecewise-linear approximated log function for compression of wide dynamic range signals. An HBT IC fabrication process based on metal-organic chemical vapor deposition (MOCVD) epitaxy and a 3 μm emitter self-aligned base ohmic transistor is used to advance the state-of-the-art log IF amplifier technology in terms of IF frequency and bandwidth, pulse resolution, and monolithic dynamic range and accuracy. The true log IF amp performance includes DC-3 GHz IF/video bandwidth, 400 pS rise time, and <±1 dB log error over ≈40 dB dynamic range at 3 GHz.

INTRODUCTION

Logarithmic amplifiers are critical components in many radar and electronic warfare (EW) applications requiring the compression of wide dynamic range signals, beyond the usefulness of linear amplification (e.g. automatic gain control). Typical applications include monopulse direction finding, electronic countermeasure (ECM) receivers, frequency discriminators, and spectrum analysis (channelizers). Logarithmic amplifiers are classified into two general types (1): 1) detector-log video amplifiers (DLVAs) in which the input to the log amp is RF detected, low frequency video and 2) log intermediate frequency (IF) amplifiers in which the input is IF downconverter from RF. Present DLVA log amps have input frequency range up to 20 GHz; the RF is detected with a tunnel or Schottky diode followed by a log video amplifier. In Log IF amplifiers, detection is performed after logging functions; the IF is presently limited to ≈2 GHz. The logarithmic conformity (error) is typically better for DLVAs, however the log IF amp has generally superior pulse characteristics and greater instantaneous input dynamic range (≈80 dB for hybrid cascaded log amps).

Bipolar transistors offer attractive advantages over field-effect transistors in differential amplifier performance critical for log amplifier applications. These include exponential-based nonlinear function, better device matching, higher transconductance and output impedance for higher gain and lower distortion, and lower 1/f noise. To date silicon bipolar transistors have been used to achieve key log amplifier functions. However, the GaAs heterojunction bipolar transistor (HBT) offers improved speed, power, and gain performance over silicon with significantly relaxed fabrication requirements. Critical emitter lithographic dimensions of ≈3 μm are adequate to achieve HBT transistors with f_t and f_{max} of 20-40 GHz. The availability of semi-insulating GaAs substrate for circuit integration is also attractive for reduced parasitic capacitance as well as simplifying device isolation. The HBT technology has already demonstrated state-of-the-art analog-to-digital conversion circuits (2,3) and microwave/millimeter-wave devices (4,5). This paper describes initial logarithmic IF amplifier results obtained with an advanced HBT fabrication process attractive for baseband/RF analog applications.

LOG IF AMPLIFIER DESIGN

In this work a true log IF amplifier was investigated using the GaAs HBT technology. Logarithmic IF conversion can be implemented as a "true" (Fig. 1) or "successive-detection" log IF (Fig. 2) amplifier when using the piecewise-linear approximation technique with cascaded stages (1). Each log

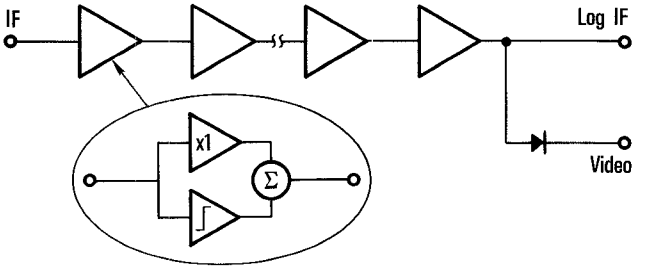

Fig. 1 True log IF amplifier with cascaded log stages (limiting/unity dual gain); carrier output is proportional to the log of the carrier input.

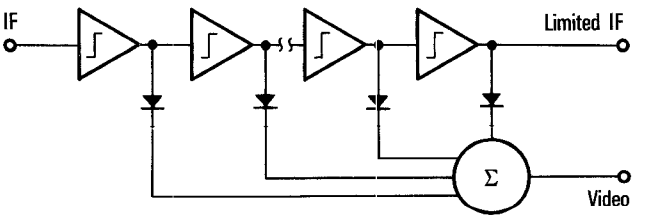

Fig. 2 Successive-detection logarithmic IF amplifier with cascaded log stages (limiting amplifiers); carrier output is proportional to the log of the detected output.

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stage utilizes a limiting amplifier, and as the input signal level increases more amplifier stages limits, and a piecewise-linear approximation to the log function is achieved. In the true log IF amp, video detection is performed after the cascaded log functions while in the successive-detection approach, detection is performed after each logging stage and the outputs summed. The true log IF amp is term "true" because the carrier output is proportional to the log of the carrier input; phase information is inherently preserved by the serial logging stages. In the successive-detection approach the carrier output is proportional to the log of the detected output; phase information is not preserved due to phase delays associated with the successive detection and summation, although it can be compensated for with delay lines. Compared to the true log IF, the successive-detection approach has less stringent dynamic range requirement on the detector; the true log IF requires video detection over the total logged dynamic range while the successive-detection requires only a fraction.

The GaAs HBT true log IF amplifier design, shown schematically in Fig. 3, is implemented as a monolithic four-stage without detection. The component log stage is based on a Si bipolar dual-gain stage design, consisting of parallel-combined limiting and unity gain amplifiers (6). The dual-gain log stage is realized with the differential HBT amplifier combination shown in Fig. 4 which are summed and DC coupled to the next stage. The total dynamic range and accuracy is determined by the number of stages and the gain of the stage. The higher the gain the greater the inaccuracy; the gain of each stage then determines the number of stages needed to achieve the dynamic range. For the HBT log IF amp, the gain of the log stage was designed as 12 dB, yielding a total 4-stage dynamic range of 48 dB. Integration of additional dual-gain stages is limited by noise and isolation considerations. To achieve a wider dynamic range

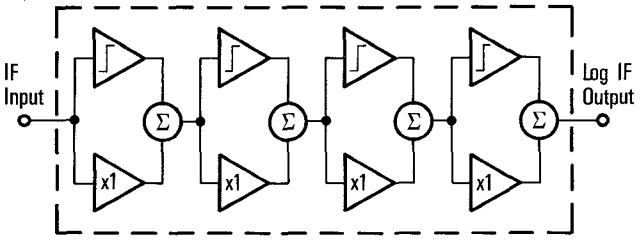

Fig. 3 Block diagram of the HBT monolithic 4-stage true log IF amplifier.

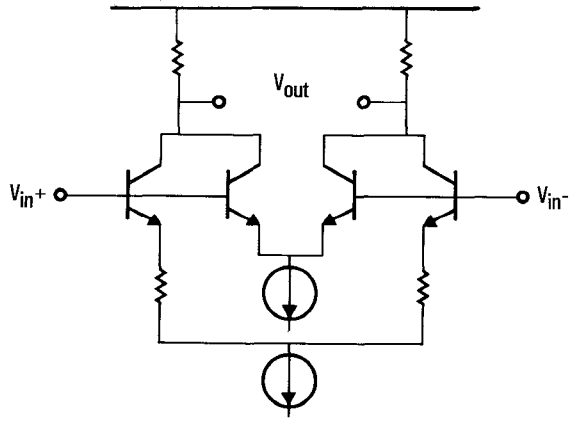

Fig. 4 Circuit schematic of the dual-gain log stage used in the HBT monolithic 4-stage true log IF amplifier.

log amp, two monolithic 4-stage log amps can be hybrid cascaded with filtering to achieve ≈80 dB dynamic range. The intrinsic HBT log amplifiers are useful from DC to ≈3 GHz, however actual log amp bandwidth within the DC-3 GHz regime is dictated by the noise (tangential signal sensitivity or TSS) requirements.

HBT LOG AMP FABRICATION TECHNOLOGY

The monolithic 4-stage true log IF amplifier was fabricated with a self-aligned base ohmic metal HBT IC process and metal-organic chemical vapor deposition (MOCVD) epitaxy specifically chosen for high performance, high-throughput/low-cost baseband/RF analog IC applications. The self-aligned HBT process and MOCVD materials are two significant changes to the previous TRW baseline HBT IC process which uses a non self-aligned transistor and molecular-beam epitaxy (MBE). The baseline process has already demonstrated high performance analog/digital conversion circuits (2,3).

MOCVD material technology offers potential advantages of higher wafer throughput and lower cost over molecular-beam epitaxial technique (MBE) with comparable performance. GaAs/AlGaAs MOCVD epitaxy is used to grow the npn HBT emitter-up, single heterostructure shown in Fig. 5. The initial HBT growth focused on a simplified structure for fabrication ease. The base layer is relatively thick and no material enhancements such as built-in drift fields or velocity overshoot structures were implemented.

The self-aligned mesa HBT IC fabrication structure (12 mask levels), shown schematically in Fig. 6, integrates key

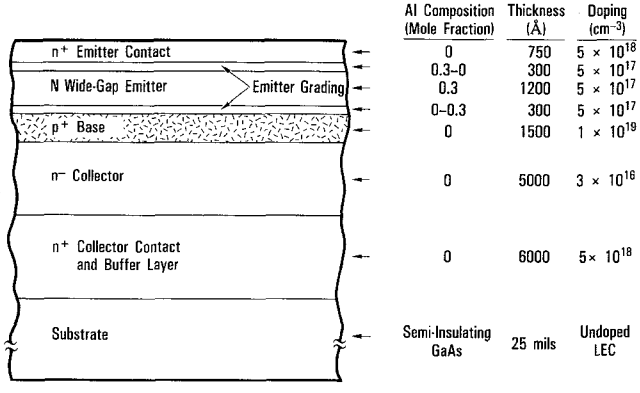

Fig. 5 Metal-organic chemical vapor deposition (MOCVD) epitaxy GaAs/AlGaAs emitter-up Npn HBT growth structure.

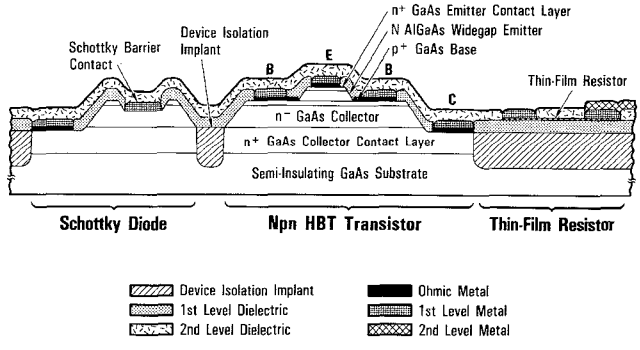

Fig. 6 Integrated circuit fabrication structure cross-section with self-aligned base ohmic metal HBT transistor, Schottky diode, and thin-film resistor.

device components including transistors, Schottky diodes, laser trimmable thin-film resistors, and metal-insulator-metal (MIM) capacitors. For the HBT, the self-aligned base metal essentially eliminates the parasitic external base resistance, by minimizing the ohmic metal to emitter spacing, to effectively double f_{max}. A double photoresist liftoff technique is used to selectively pattern the HBT base ohmic metal to within ≈0.1 μm of the emitter edge. The active device layers are accessed by a combination of selective and non-selective wet chemical etches. Ohmic contacts are formed by AuBe/Pd/Au and AuGe/Ni/Ti/Au for p-type and n-type ohmic contacts, respectively. A multiple boron damage implant is used for device isolation. Plasma-enhanced CVD silicon nitride is used to passivate the GaAs surface and serves as a dielectric insulator for MIM hold capacitors and double-level metal interconnection (TiPtAu and TiAu). TiPtAu used as the first interconnect metal also serves as the Schottky barrier metal.

The standard HBT device uses a 3x10 μm^2 emitter-base junction. For such devices, the MOCVD fabrication process demonstrates excellent transistor DC and RF characteristics as shown in Figs. 7 and 8, respectively. The DC current gain ß≈30 (I_C=1 mA) is about a factor of 2-3 lower than MBE material, but is still useful for analog applications. The f_t and f_{max}≈15-25 GHz (I_C≈1mA) are about 10-20 percent lower than the equivalent MBE structure but adequate for >3 GHz IF analog IC applications as demonstrated by the 6 GHz (40 mW) divide-by-2 prescaler shown in Figs. 9-11. The lower MOCVD performance compared to MBE is believed to be associated with non-optimized epitaxial growth, including base dopant diffusion effects and reduced emitter doping. Both the DC ß and f_t, f_{max} can be improved by reducing the base thickness (by a factor of 2) from the relaxed 1500 Å currently used. Work is in progress to further refine the MOCVD HBT growth structure.

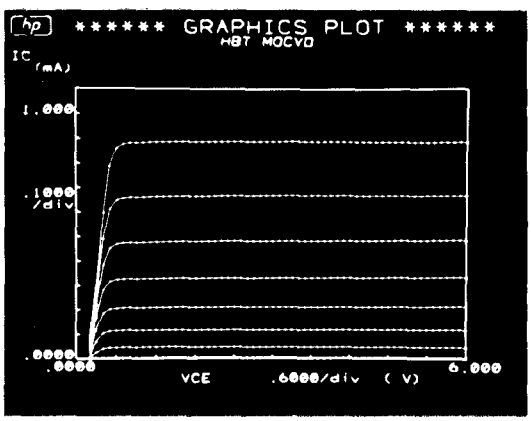

Fig. 7 IV characteristic of MOCVD 3x10 μm^2 emitter, self-aligned base metal HBT; ß≈30 @ I_C≈1 mA
(V: 0.1 mA/div; H: 0.6 V/div; ΔI_b=4 μA).

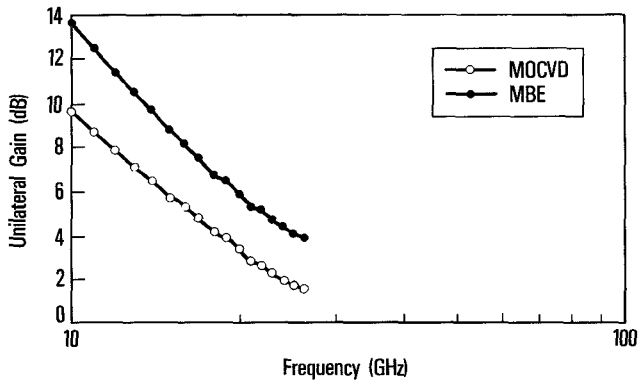

Fig. 8 Comparison of MOCVD and MBE for 3x10 μm^2 HBT (I_C≈5 mA) unilateral gain (derived from S parameters); MOCVD f_{max}≈30 GHz, MBE f_{max}≈43 GHz).

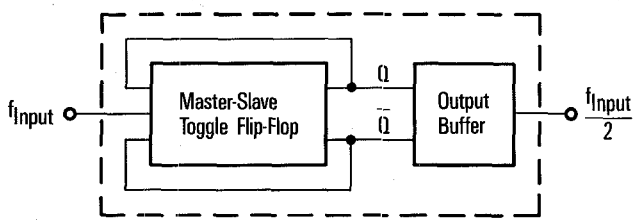

Fig. 9 Divide-by-2 prescaler block diagram.

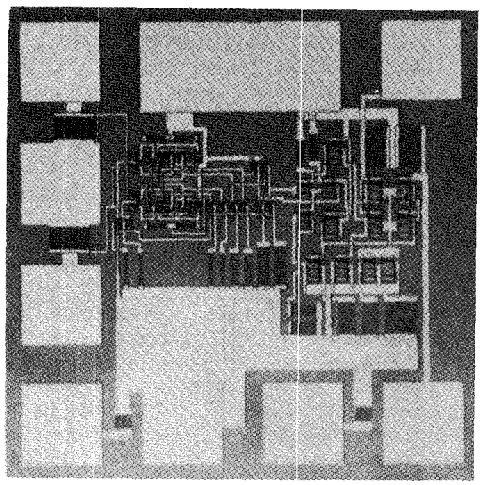

Fig. 10 Photo of fabricated divide-by-2 prescaler using MOCVD epitaxy and self-aligned base metal HBTs (39 transistors; chip size: 0.55 mm x0.55 mm).

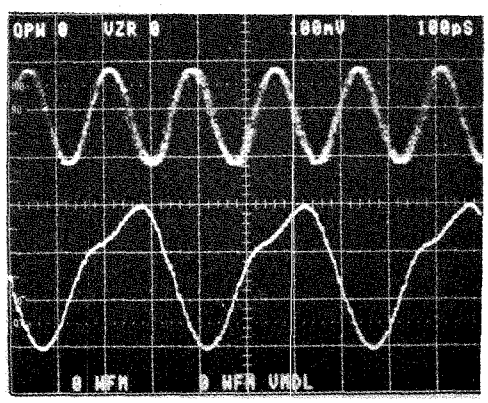

Fig. 11 Divide-by-2 prescaler with input at 6 GHz (40 mW)
(V: 100 mV/div; H: 100 pS/div).

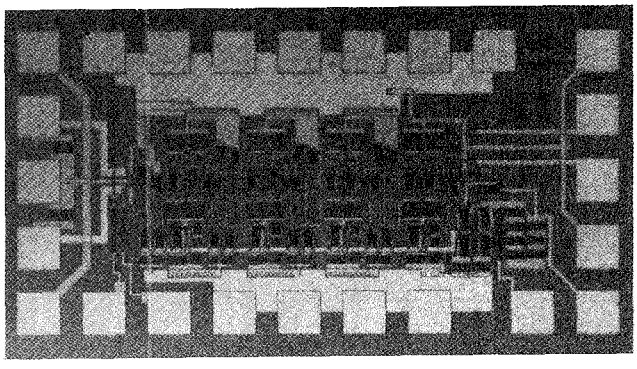

Fig. 12 Photo of fabricated monolithic 4-stage true log IF amplifier using MOCVD epitaxy and self-aligned base metal HBTs (45 transistors; chip size: 0.7 mmx1.25 mm).

TRUE LOG IF AMPLIFIER PERFORMANCE

The fabricated HBT log IF amplifier circuit using the MOCVD self-aligned base metal HBT IC process is shown in Fig. 12. It consists of 45 HBTs and occupies a die size of 0.7 mm x1.25 mm. All testing was performed on-wafer using 50 Ω ceramic blade probe cards. Key log amp performance parameters evaluated include the frequency and pulse response, log transfer characteristics, and log conformity (error) over the full dynamic range. The noise or tangential signal sensitivity (TSS) asssociated with the actual log bandwidth was not evaluated. The circuit uses a single supply voltage of -8 volts at 133 mA, thus dissipating 1.06 watts.

The frequency response was characterized by using a synthesized signal generator for the source and a power meter to measure the output. The log amp has an input impedance of 50 Ω and an output impedance of 100 Ω. Since the power meter has a 50 Ω input impedance and is single ended, the absolute gain of the log amp is reduced -15.56 dB. An example of the signal log compression is shown in Fig. 13 for two input power levels (0 dBm and -35 dBm) at 50 MHz. The true log IF amplifer response to a 3 GHz input at +12 dBm is shown in Fig. 14 while Fig. 15 shows the output response versus frequency over ≈3 GHz bandwidth. The peaking in the log response is due to probe blade inductance. The -3 dB frequency of a log amplifier is the frequency at which the output falls to a level equivalent to a 3 dB lower input. For the HBT log IF amplifier, the -3 dB frequency is 3 GHz.

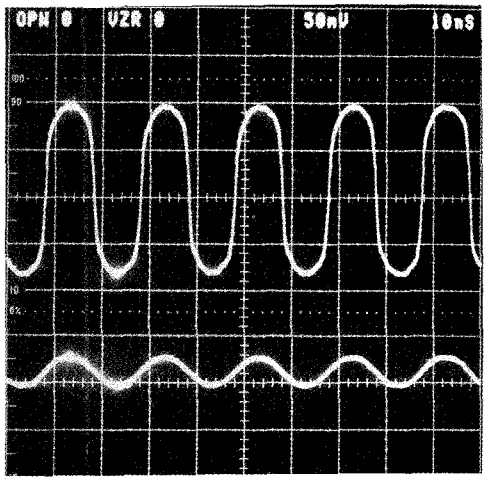

Fig. 13 Log IF amp output voltage versus input power for 0 dBm (Top) and -35 dBm (Bottom)
f_{in}= 50 MHz (V: 50 mV/div; H: 10 nS/div).

The logarithmic transfer function and log conformity (linearity or error) is derived from the input power versus output voltage transfer curves as shown in Fig. 16 for various input frequency signals. From these curves a linear

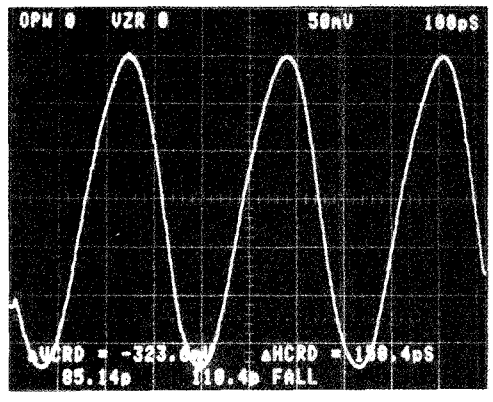

Fig. 14 Log IF amp output voltage versus input power at 12 dBm, f_{in}=3 GHz (V: 50 mV/div; H: 100 pS/div).

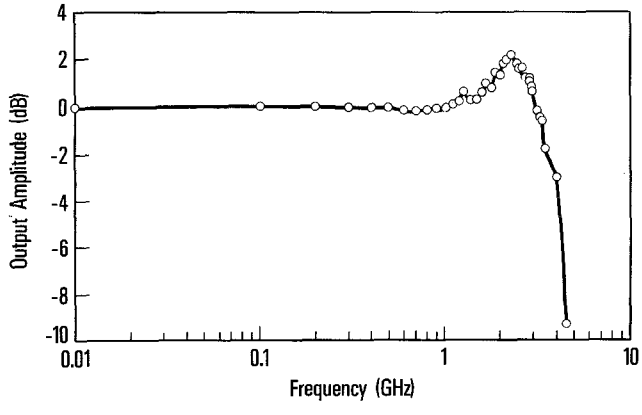

Fig. 15 Log IF amplifier output amplitude frequency response.

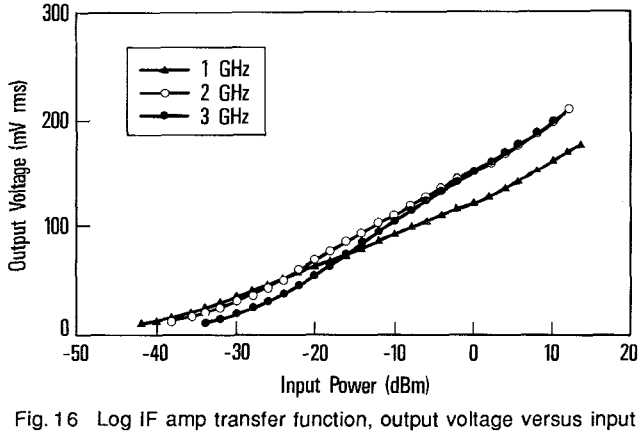

Fig. 16 Log IF amp transfer function, output voltage versus input power.

regression of input power versus output voltage is determined and subtracted from the actual measured transfer curve. This difference is input referred and is a measure of the logarithmic conformity. Figure 17 shows the log linearity versus input power from 1-3 GHz. At 1 GHz the log amp has 44 dB dynamic range, maintaining <±0.85 dB log error error while at 3 GHz the log amp has ≈40 dB dynamic range with <±1 dB log error. The dynamic range and log error designed was 48 dB and ± 1 dB. The actual dynamic range was reduced since the entire log amp is DC coupled. Any DC offset in the differential transistor pairs will be amplified by the log amp, reducing the total dynamic range. The log error is better than predicted since the log amp was designed assuming linear-limiting amplifiers. Differential pairs without emitter degeneration will have a non-linear (pseudo-logarithmic) transfer function which will reduce the log error.

The pulse response of a conventional logarithmic amplifier is specified by the rise, fall, settling, and recovery times of the detected video output. These response times are limited by the video bandwidth. A typical logarithmic amplifier has a video bandwidth which is limited by the log amp circuit bandwidth and noise requirements. The video bandwidth limits the log amp rise and fall times. If the input rise and fall times are long, then the corresponding output rise and fall times will be even longer. The fall time will require several time contants to fall within 1 dB of the corresponding minimum input signal. The 4 stage true log IF amp was tested as a log video amplifier with a 3 GHz bandwidth. A pulse with 0.4 nS rise and fall times was used as the input, yielding an output with 0.4 nS rise and 3.2 nS fall times as shown in Fig. 18. This demonstrates the capability for very narrow pulse operation.

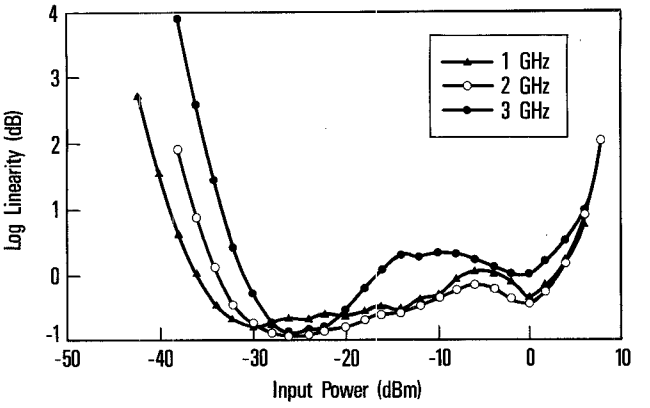

Fig. 17 Log IF amp log linearity or error versus input power.

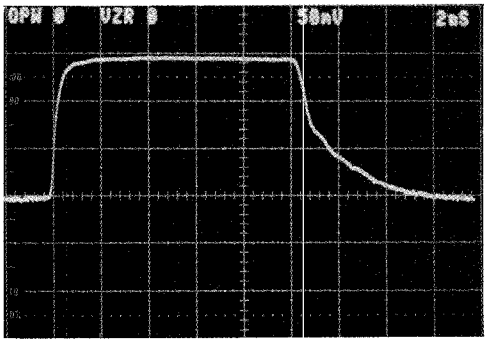

Fig. 18 Log IF amp pulse response, f_{in}= 10 nS pulse, 400 pS rise and fall time (V: 50 mV/div; H: 2 nS/div).

SUMMARY AND CONCLUSIONS

The first GaAs/AlGaAs HBT logarithmic amplifier has been demonstrated advancing the state-of-the-art performance. A monolithic 4-stage true logarithmic IF amplifier was implemented using a Si bipolar building block log amp design. The log IF amplifier was fabricated with an advanced HBT fabrication process based on MOCVD epitaxy and self-aligned base ohmic metal transistors designed for high performance and high-throughput/low-cost baseband/RF analog IC applications. Initial results have demonstrated the highest IF input frequency capability ≈3 GHz and lowest power consumption ≈1 W for a monolithic dynamic range of ≈40 dB and log error <±1 dB with operating bandwidth of ≈DC to 3 GHz and very narrow pulse resolution. These results verify the capability of the HBT technology to advance the performance beyond that of Si bipolar transistors in baseband/RF analog ICs and to utilize the potentially high-throughput/low-cost MOCVD epitaxial materials. Refined fabrication and circuit designs are expected to yield log IF amplifers with even greater performance improvements.

ACKNOWLEDGMENTS

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